ABSTRACT OF THE DISCLOSURE

There is disclosed a data processing apparatus which can reduce fanout load of a control signal for controlling a pipeline. The data processing apparatus of the present invention includes a first pipeline processing portion for executing a processing in five divided stages, a second pipeline processing portion for executing a processing one stage behind the first pipeline processing portion, and a plurality of flip-flops for latching the control signals inputted to the respective stages. The second pipeline processing portion performs the processing in each stage based on delayed control signals Control-A to E generated by once latching the control signals Control-A to E inputted to the respective stages by the flip-flop. Because of this, the fanout load of the control signals Control-A to E is reduced, and signal delay of the control signals Control-A to E can be reduced. Moreover, a wiring length of a control line for transmitting the control signals Control-A to E can be set to be longer than a conventional wiring length.